AXS2045

2x40W D

AXS2045 2x40W D

BTL

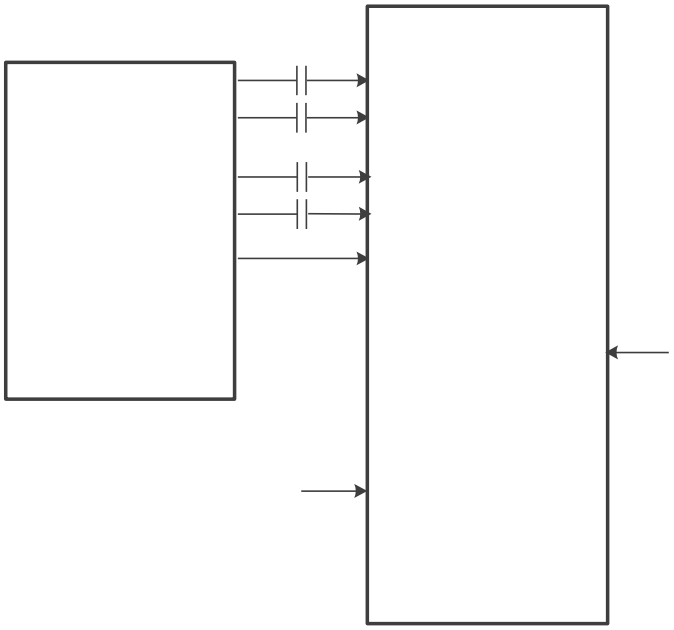
4- 8 Ω PBTL 2- 4 Ω

PSRR

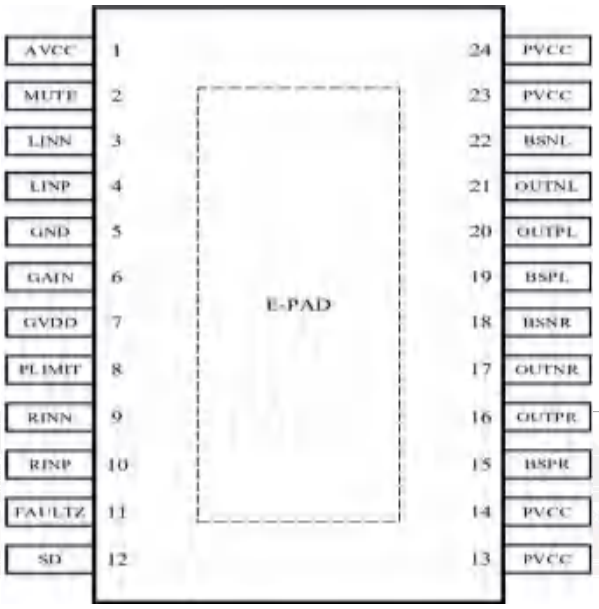
- 5V 26V
- 20dB 26dB 32dB
- D

  BTL 2x20W 4 Ω 10%THD+N 12V
  BTL 2x40W 8 Ω 10%THD+N 24V
  BTL 2x55W 4 Ω 1% THD+N24V
  PBTL 1x80W 3 Ω 1%THD+N 24V

AXS2045 ETSSOP24 E-PAD



Pin Configuration and Functions



PIN	TYPE

Order Information

Part Number	Package Type	Marking	Package Qty	Temp Range (℃)
AXS2045				



4. Thermal Information

THERMAL METRIC		AXS2045 24 PINS	UNIT
R_{JA}	Junction-to-ambient thermal resistance	22	°C/W
$_{JT}$	Junction-to-top characterization parameter	0.3	°C/W
$_{JB}$	Junction-to-board characterization parameter	4.8	°C/W

For the PCB layout, see the AXS2045EVM user guide.

5. DC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω, f_s = 400 kHz, hybrid mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V		1.5	5	mV
I_{CC}	Quiescent supply current	SD = 2 V, With load and filter, PV_{CC} = 12 V		12		mA
		SD = 2 V, With load and filter, PV_{CC} = 24 V		18		
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SD = 0.8 V, With load and filter, PV_{CC} = 12 V		20		μA
		SD= 0.8 V, With load and filter,				

7. Typical Characteristics

f_s = 400kHz(unlessotherwisenoted)



Typical Charac 0 0 9 1fact <</Attached [/Bottom]/Type/Pa26081(h)9(ar)17(ac)16(t) 1B0 0 0 9 1fact <</Attached [/Bottom]/Typ

Typical Characteristics (continued)

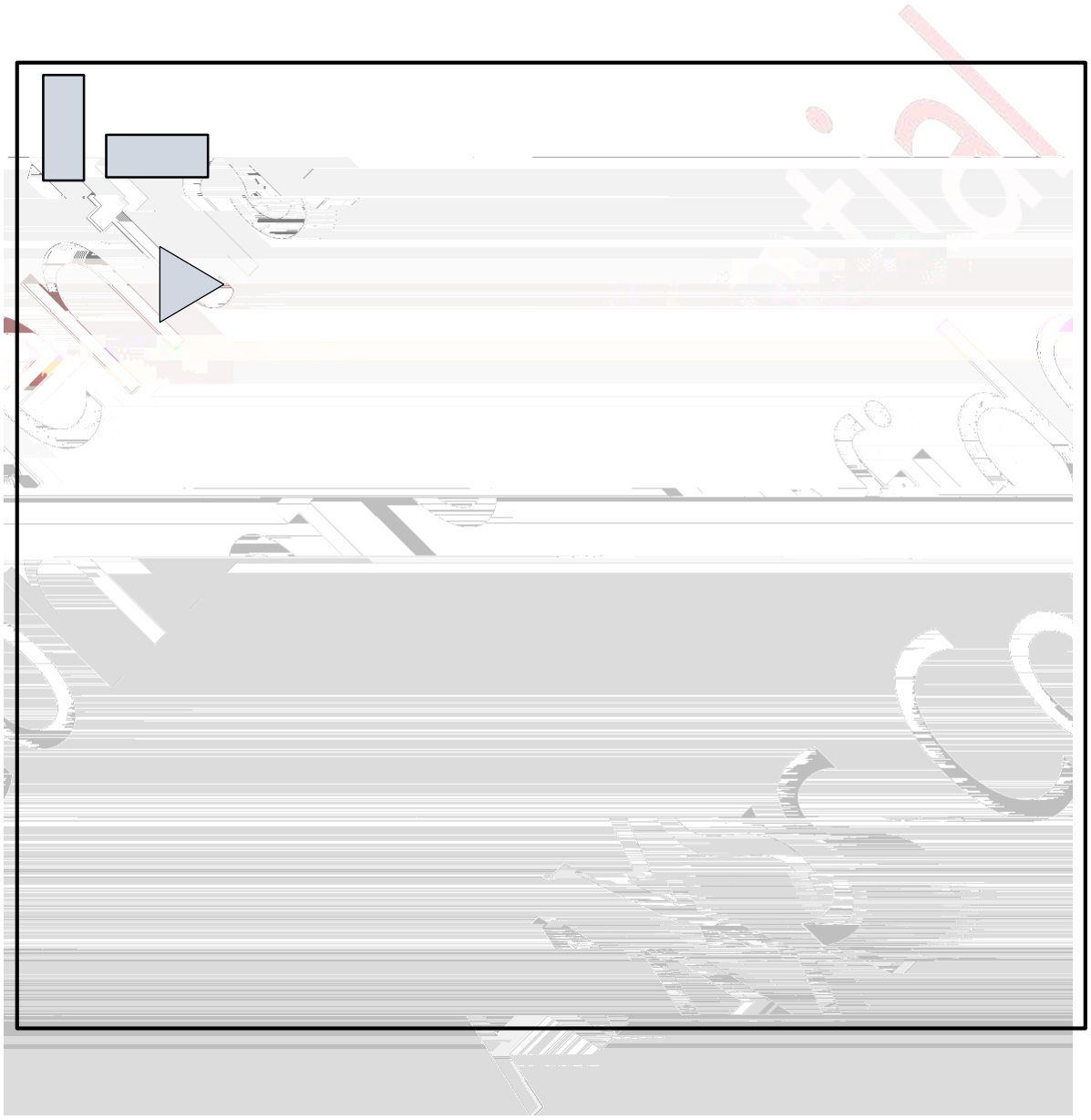
f_s = 400 kHz (unless otherwise noted)

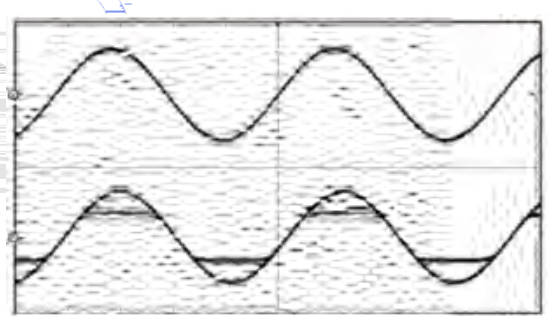


Typical Characteristics (continued)

f_S = 400 kHz, (unless otherwise noted)







The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

where

P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

R_L is the load resistance.

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.

V_P is the peak amplitude, which is limited by the "virtual" voltage rail.

3. Power Limit Example

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Open	Short	17.9
24 V	3.3	45 k	51 k	12.67
24 V	2.25	24 k	51 k	9
12 V	GVDD	Open	Short	10.33
12 V	2.25	24 k	51 k	9
12 V	1.5	18 k	68 k	6.3

PLIMIT measurements taken with EVM gain set to 26 dB and input voltage set to 1 V_{rms}.

8.3.5 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. The GVDD supply can also be used to supply the PLIMIT and GAIN voltage dividers. Decouple GVDD with a X5R ceramic 1-µF capacitor to GND. The GVDD supply is not intended to be used for external supply.

The current consumption should be limited by using resistor voltage dividers for GAIN and PLIMIT of 100 N R U P R U H

8.3.6 BSPx and BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to the corresponding bootstrap input. ed] TJ ET Q q 0.0000

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10.3.2 Select Input Capacitance

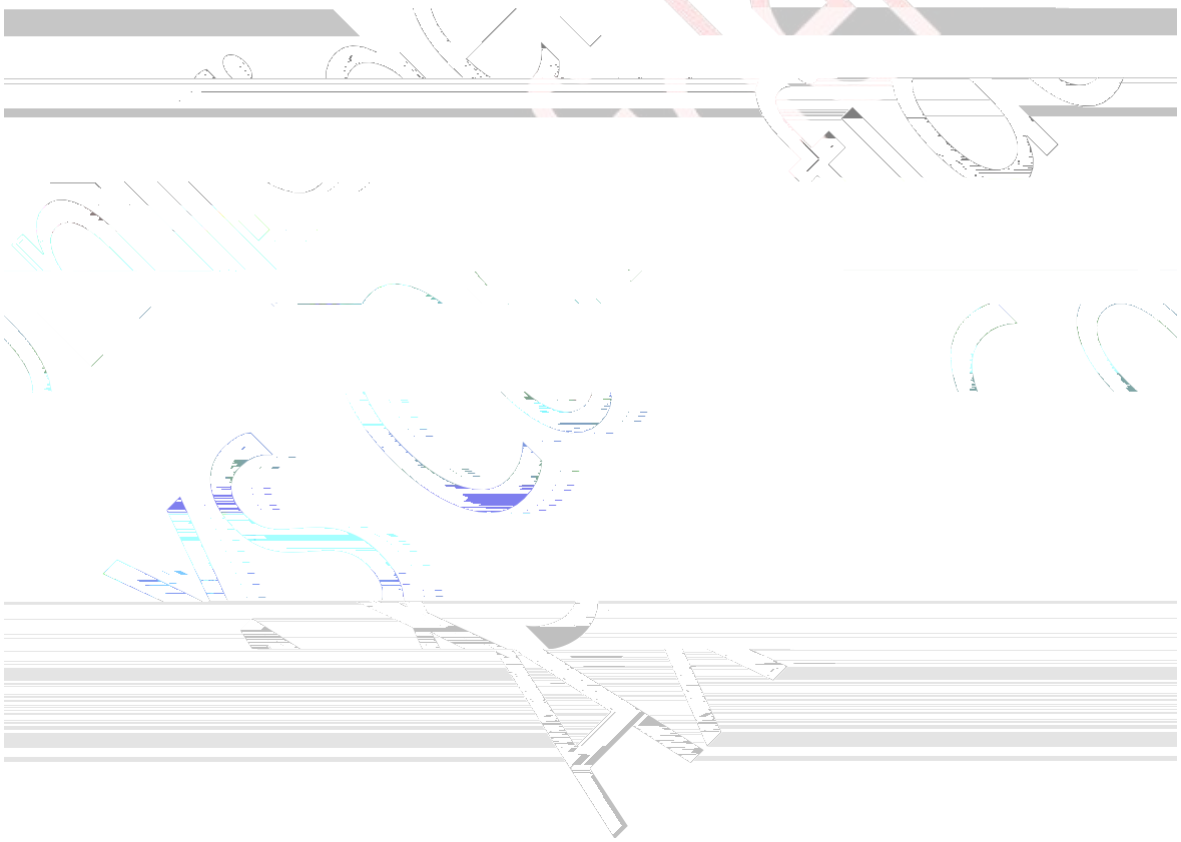
Select the bulk capacitors at the PVCC inputs for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed power supply, two 220 F/50V capacitors should be sufficient. One capacitor should be placed near the PVCC inputs at each side of the device. PVCC capacitors should be a low ESR type because they are being used in a fast-switching application.

10.3.3 Select Decoupling Capacitors

Good quality decoupling capacitors must be added at each of the PVCC inputs to provide good reliability, audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVCC and GND connections to the device in order to minimize series inductances.

10.3.4 Select Bootstrap Capacitors

Each of the outputs require bootstrap capacitors to provide the outputs 595.56 842.04 re W* n BT /F2 9.96 Tf 1 0 0 1 295.5

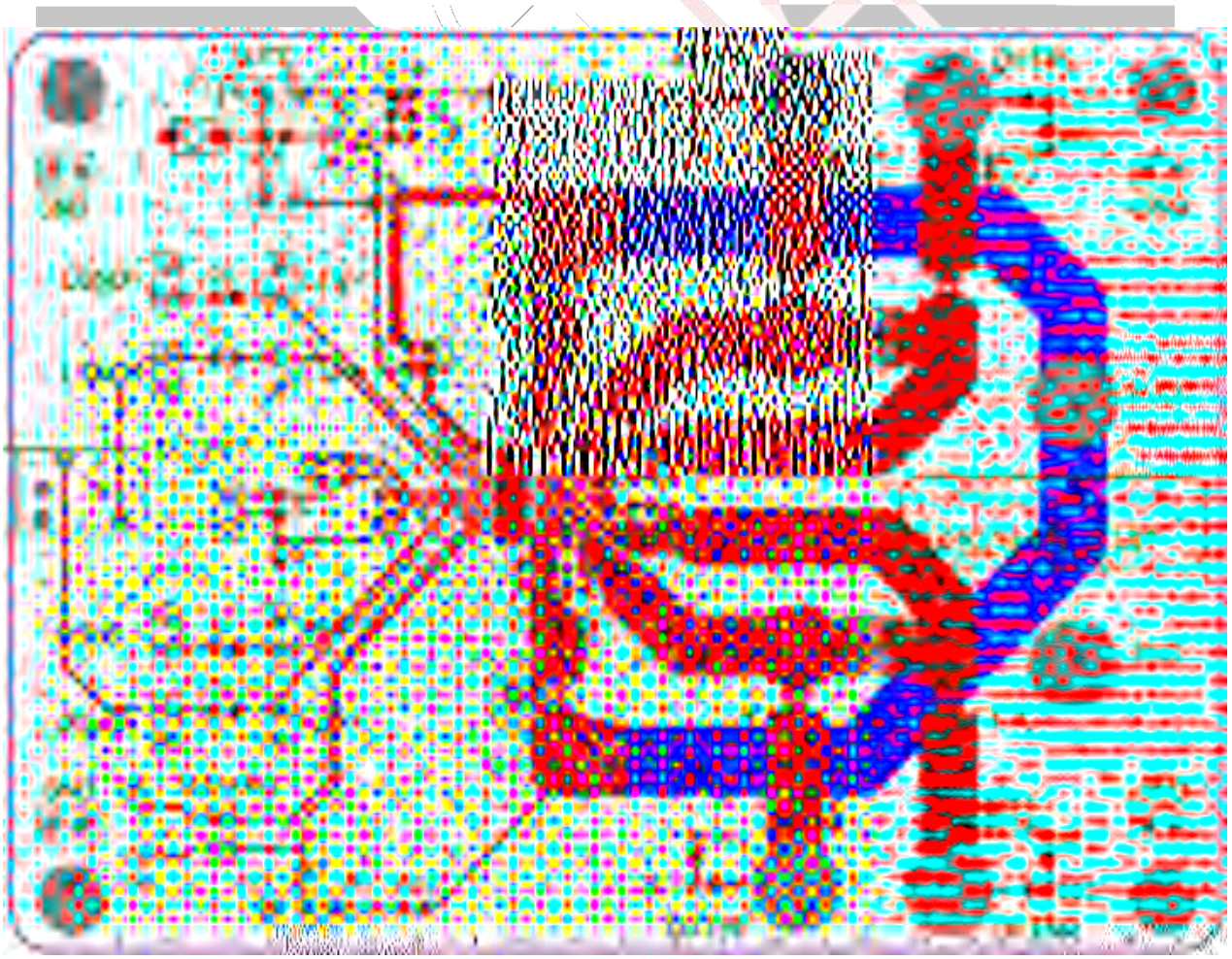


decoupling capacitors should be placed near the AXS2045 on the PVCC supplies. Local, high-frequency bypass (0.1μF) should be placed as close as possible to the PVCC pins. The PVCC

The size of this current loop determines its effectiveness as an antenna.

- Grounding † The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the AXS2045.
- Output filter † The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

10.3.8 Layout Example



ETSSOP24

